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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/057,098	01/23/2002	Pingxi Ma	01CON356P	2773

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EXAMINER
NGUYEN, KHANH V

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/057,098	MA ET AL.	
	Examiner	Art Unit	
	Khanh V. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-5, 7, 8, 10, 11, 14, 16, 18-22, 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Hageraats (6,204,728).

Regarding claim 1, Hageraats (Fig. 4B) discloses an RF amplifier with distortion reduction comprising: a bipolar transistor (70); a field effect transistor (72); the base of bipolar transistor (70) coupled to input (36); the emitter (44) of bipolar transistor (70) coupled to a first reference voltage (46); the collector of bipolar transistor (70) coupled to the source of field effect transistor (72); the gate of the field effect transistor coupled to bias voltage (Vbias); the drain of the field effect transistor (72) coupled to a second reference voltage (50); and the drain of the field effect transistor (72) coupled to output (38).

Regarding claim 14, Hageraats (Fig. 4B) discloses an RF amplifier with distortion reduction, wherein the RF amplifier can be read as BiFET (bipolar+field effect transistor)

low noise amplifier comprising: a bipolar transistor (70); a field effect transistor (72); the base of bipolar transistor (70) coupled to input (36); the emitter (44) of the bipolar transistor (70) coupled to the first reference voltage (46) through a first impedance circuit (42); the collector of bipolar transistor (70) coupled to the source of field effect transistor (72); the gate of the field effect transistor coupled to bias voltage (Vbias); the drain of the field effect transistor (72) coupled to a second reference voltage (50) through a second impedance circuit (48 and Co); and the drain of the field effect transistor (72) coupled to output (38).

Regarding claims 2, 3, 18, wherein the emitter (44) of the bipolar transistor (70) coupled to the first reference voltage (46) through a first impedance circuit (42), wherein the first impedance circuit (42) comprises an inductor (Lse).

Regarding claims 4, 5, 19, wherein the drain of the field effect transistor (72) coupled to the second reference voltage (50) through a second impedance circuit, wherein the second impedance circuit comprises an inductor (48/Lcc) and a capacitor (Co).

Regarding claims 7, 16, wherein the field effect transistor (72) is an N-channel FET.

Regarding claim 8, wherein the bipolar transistor (70) coupled to the field effect transistor (72) in cascode configuration in BiFET/BICMOS low noise amplifier (see col. 5, lines 59-64).

Regarding claims 10, 20, wherein the capacitor (Co) is coupled to the drain of field effect transistor (72).

Regarding claims 11, 21, wherein the inductor (Lcc) coupled to the drain of field effect transistor (72) to the second reference voltage (50).

Regarding claim 22, wherein the capacitor (Co) coupled to the drain of field effect transistor (72) to the output (38).

Regarding claim 24, wherein an RF signal is inputted to the base of the bipolar transistor (70).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6, 9, 13, 15, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hageraats (6,204,728).

Regarding claims 6, 15, Hageraats (Fig. 4B) discloses the claimed invention but fails to mention the semiconductor technology called SiGe. Hageraats utilizes heterojunction bipolar transistor in general. However, since in any practical use of the invention some type of semiconductor technologies would be used and utilization of such known technologies (SiGe ...) would have been obvious matter of design choice in the absence of unexpected results.

Regarding claims 9, 17, Hageraats (Fig. 4B) discloses the claimed invention except the first reference voltage is ground voltage. Hageraats utilizes a low voltage reference (Vlow, ref). It would have been an obvious matter of design choice to have replaced low voltage reference (Vlow, ref) with a ground voltage, since applicant has not disclosed that a ground voltage solves any stated problem or is for any particular purpose and in light of any criticality or unexpected result it appears that the invention would perform equally well with low voltage reference (Vlow, ref) grounded.

Regarding claim 13, Hageraats (Fig. 4B) discloses the claimed invention except the second reference voltage is Vdd. Hageraats utilizes a high voltage reference (Vhigh, ref). It would have been an obvious matter of design choice to have replaced high voltage reference (Vhigh, ref) with Vdd, since applicant has not disclosed that Vdd solves any stated problem or is for any particular purpose and in light of any criticality or unexpected result it appears that the invention would perform equally well with Vdd.

Claims 12, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hageraats in view of Pickett (4,754,233).

Hageraats (Fig. 4B) discloses the claimed invention except an input capacitor coupled between the input and the base of the bipolar transistor.

Pickett (Fig. 2) discloses an input capacitor (32) coupled between input (13) and a base of bipolar transistor (36) for DC blocking.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have modified the circuit of Hageraats to have included an input capacitor coupled between the input and the base of a bipolar transistor, as exemplarily taught by Pickett. Such, as modification would have imparted the advantageous benefit of provide DC blocking to the base of the bipolar transistor (see col. 2, lines 53-55) as taught by Pickett, to Hageraats reference, thereby suggesting the obviousness of such a modification.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additional reference (Osawa (4,528,520)) shows further analogous prior art circuitry (bipolar and FET connected in cascode).

This art is deemed relevant and should be carefully reviews before any amendment is filed.

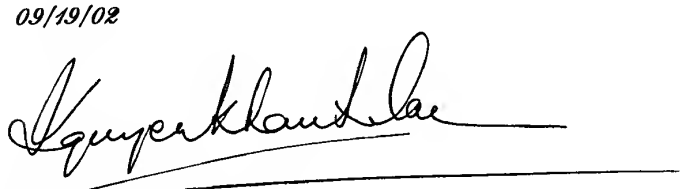
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh V. Nguyen whose telephone number is (703) 306-9058. The examiner can normally be reached from 8:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service at (703) 872-9317.

NKV

09/19/02



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Group 2800, Art Unit 2817